

CLAIMS

What is claimed is:

1. An assembly having multiple substrates and a plurality of semiconductor dice located on said multiple substrates, comprising:
 - a base substrate having a first surface including a plurality of bond pads and a plurality of circuits connected to said plurality of bond pads;
 - at least one first semiconductor die having an active surface having at least one bond pad thereon and having a second surface;
 - a first stacked substrate having a first surface, having a second surface, and having a plurality of circuits, said at least one first semiconductor die electrically connected to said first surface of said first stacked substrate and having said second surface thereof disposed on at least one portion of said first surface of said first stacked nonconductive substrate;
 - at least one second semiconductor die having a first surface having a plurality of bond pads located thereon, said first surface of said at least one second semiconductor die attached to at least one portion of said second surface of said first stacked substrate;
 - at least one first connector connecting said at least one bond pad of said at least one first semiconductor die to at least one bond pad of said plurality of bond pads of said base substrate;
 - at least one second connector connecting at least one bond pad of said plurality of bond pads of said at least one second semiconductor die to at least one other bond pad of said plurality of bond pads of said base substrate;
 - a second stacked substrate having a first surface, having a second surface, and having a plurality of circuits;
 - at least one third semiconductor die having a first surface having a plurality of bond pads located thereon, said first surface of said at least one third semiconductor die attached to at least one portion of said first surface of said second stacked nonconductive substrate; and

at least one third connector connecting at least one bond pad of said plurality of bond pads of said at least one third semiconductor die to said first surface of said first stacked substrate.

2. The assembly of claim 1, wherein said at least one first semiconductor die is located on a portion of said first surface of said first stacked substrate being electrically connected to said first stacked substrate thereat.

3. The assembly of claim 1, wherein said second surface of said first stacked nonconductive substrate includes a plurality of bond pads; and wherein said at least one second semiconductor die is located on and electrically connected to said portion of said second surface of said first stacked substrate.

4. The assembly of claim 1, wherein said at least one first connector includes one of solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

5. The assembly of claim 1, wherein said base substrate further comprises a second surface having a plurality of bond pads located thereon.

6. The assembly of claim 5, further comprising connections attached to said plurality of bond pads of said second surface of said base substrate for connection with external electrical circuitry.

7. The assembly of claim 6, further comprising a plurality of trace leads located on said base substrate connecting said plurality of bond pads of said first surface of said base substrate and said plurality of bond pads of said second surface of said base substrate.

8. The assembly of claim 1, further comprising:
a base semiconductor die having a plurality of bond pads and disposed on said base substrate first surface; and
at least one fourth connector connecting said at least one of said plurality of bond pads of said first surface of said base substrate and said at least one bond pad of said at least one first semiconductor die.

9. An assembly having a plurality of substrates and having a plurality of semiconductor dice comprising:
a base substrate having a first surface including a plurality of bonds pads thereon, a second surface including a plurality of bond pads thereon, and a plurality of traces, at least one trace of said plurality of traces connecting at least one bond pad of said plurality of bond pads on said first surface of said base substrate to at least one bond pad of said plurality of bond pads on said second surface of said base substrate;
a first stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces connecting at least one bond pad of said plurality of bond pads on said first surface of said first stacked substrate to at least one bond pad of said plurality of bond pads on said second surface of said first stacked substrate, and a second plurality of traces, at least one trace of said second plurality of traces connected to another bond pad of said plurality of bond pads on said first surface of said first stacked substrate;
a first semiconductor die disposed on said first surface of said first stacked substrate, said first semiconductor die connected to said at least one trace of said second plurality of traces connected to said another bond pad of said plurality of bond pads on said first surface of said first stacked substrate;
a second stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces of said second stacked nonconductive

substrate connecting at least one bond pad of said plurality of bond pads on said first surface of said second stacked substrate to at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate, and a second plurality of traces, at least one trace of said second plurality of traces of said second stacked substrate connected to another bond pad of said plurality of bond pads on said first surface of said second stacked substrate;

a second semiconductor die disposed on said first surface of said second stacked substrate, said second semiconductor die connected to said at least one trace of said second plurality of traces of said second stacked nonconductive substrate connected to said another bond pad of said plurality of bond pads on said first surface of said second stacked substrate;

a third semiconductor die disposed on said second surface of said second stacked substrate;

a first plurality of connections connecting said base substrate and said first stacked substrate, at least one connection of said first plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said base substrate to said at least one bond pad of said plurality of bond pads on said first surface of said first stacked substrate, said first plurality of connections connecting said base substrate and said first stacked substrate supporting said first stacked substrate;

a second plurality of connections connecting said second stacked substrate and said first stacked substrate, at least one connection of said second plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said second stacked substrate to said at least one bond pad of said plurality of bond pads on said second surface of said first stacked substrate, said second plurality of connections connecting said first stacked substrate and said second stacked substrate supporting said second stacked substrate;

a third stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces of said third stacked nonconductive substrate connecting at least one bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate to at least one bond pad of said

plurality of bond pads on said second surface of said third stacked substrate, and a second plurality of traces, at least one trace of said second plurality of traces of said third stacked substrate connected to another bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate;

a fourth semiconductor die disposed on said second surface of said third stacked nonconductive substrate;

a fifth semiconductor die disposed on said first surface of said third stacked nonconductive substrate, said fifth semiconductor die connected to said at least one trace of said second plurality of traces of said third stacked nonconductive substrate connected to said another bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate; and

a third plurality of connections connecting said third stacked nonconductive substrate and said second stacked substrate, at least one connection of said third plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate.

10. The assembly of claim 9, wherein said first plurality of connections includes solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

11. The assembly of claim 9, wherein said second plurality of connections includes solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

12. The assembly of claim 9, further comprising:

a fourth plurality of connections, at least one connection of said fourth plurality of connections connecting said at least one bond pad of said plurality of bond pads on said second surface of said base substrate to external electrical circuitry.

13. The assembly of claim 9, wherein said first semiconductor die disposed on said first surface of said first stacked substrate is connected to said at least one trace of said second plurality of traces connected to said another bond pad of said plurality of bond pads on said first surface of said first stacked substrate through one of flip chip attachment, wirebonding, TAB tape, and a combination thereof.

14. The assembly of claim 9, wherein said second semiconductor die disposed on said first surface of said second stacked substrate is connected to said at least one trace of said second plurality of traces of said second stacked substrate connected to said another bond pad of said plurality of bond pads on said first surface of said second stacked substrate through one of flip chip attachment, wirebonding, TAB tape, and a combination thereof.

15. The assembly of claim 9, wherein said third semiconductor die disposed on said second surface of said second stacked substrate is connected to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate.

16. The assembly of claim 9, wherein said third semiconductor die disposed on said second surface of said second stacked substrate is connected to said at least one bond pad of said plurality of bond pads on said first surface of said second stacked substrate.

17. The assembly of claim 9, wherein said second semiconductor die disposed on said first surface of said second stacked substrate is connected to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate and wherein said third semiconductor die disposed on said second surface of said second stacked substrate is connected to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate.

18. The assembly of claim 9, further comprising:

- a fourth stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces of said fourth stacked substrate connecting at least one bond pad of said plurality of bond pads on said first surface of said fourth stacked substrate to at least one bond pad of said plurality of bond pads on said second surface of said fourth stacked substrate, and a second plurality of traces, at least one trace of said second plurality of traces of said fourth stacked substrate connected to another bond pad of said plurality of bond pads on said first surface of said fourth stacked nonconductive substrate, said fourth stacked substrate located above said second stacked substrate, said fourth stacked substrate having a size less than sizes of said base substrate, said first stacked substrate, said second stacked substrate, and said third stacked nonconductive substrate;
- a sixth semiconductor die disposed on said first surface of said fourth stacked substrate, said sixth semiconductor die connected to said at least one trace of said second plurality of traces of said fourth stacked substrate connected to said another bond pad of said plurality of bond pads on said first surface of said fourth stacked substrate; and
- a fourth plurality of connections connecting said fourth stacked substrate and said second stacked substrate, at least one connection of said fourth plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said fourth stacked substrate to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked substrate.

19. An assembly having a plurality of substrates and having a plurality of semiconductor dice comprising:

- a base substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, and a plurality of traces, at least one trace of said plurality of traces connecting at least one bond pad of said plurality of bond pads on said first surface of said base substrate to at least one bond pad of said plurality of bond pads on said second surface of said base substrate;
- a first stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces connecting at least one bond pad of said plurality of bond pads on said first surface of said first stacked substrate to at least one bond pad of said plurality of bond pads on said second surface of said first stacked substrate, and a second plurality of traces, at least one trace of said second plurality of traces connected to another bond pad of said plurality of bond pads on said first surface of said first stacked substrate;
- a plurality of first semiconductor dice disposed on said first surface of said first stacked substrate, each die of said plurality of first semiconductor dice connected to said at least one trace of said second plurality of traces connected to said another bond pad of said plurality of bond pads on said first surface of said first stacked substrate;
- a second stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces of said second stacked nonconductive substrate connecting at least one bond pad of said plurality of bond pads on said first surface of said second stacked nonconductive substrate to at least one bond pad of said plurality of bond pads on said second surface of said second stacked nonconductive substrate, and a second plurality of traces, at least one trace of said second plurality of traces of said second stacked nonconductive substrate connected to another bond pad of said plurality of bond pads on said first surface of said second stacked nonconductive substrate;

a plurality of second semiconductor dice disposed on said first surface of said second stacked nonconductive substrate, each die of said plurality of second semiconductor dice connected to said at least one trace of said second plurality of traces of said second stacked nonconductive substrate connected to said another bond pad of said plurality of bond pads on said first surface of said second stacked nonconductive substrate;

a plurality of third semiconductor dice disposed on said second surface of said second stacked nonconductive substrate;

a first plurality of connections connecting said base substrate and said first stacked substrate, at least one connection of said first plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said base substrate to said at least one bond pad of said plurality of bond pads on said first surface of said first stacked substrate, said first plurality of connections connecting said base substrate and said first stacked substrate supporting said first stacked substrate;

a second plurality of connections connecting said second stacked nonconductive substrate and said first stacked substrate, at least one connection of said second plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said second stacked nonconductive substrate to said at least one bond pad of said plurality of bond pads on said second surface of said first stacked substrate;

a third stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of said first plurality of traces of said third stacked nonconductive substrate connecting at least one bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate to at least one bond pad of said plurality of bond pads on said second surface of said third stacked nonconductive substrate, and a second plurality of traces, at least one trace of said second plurality of traces of said third stacked nonconductive substrate connected to another bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate;

a plurality of fourth semiconductor dice disposed on said first surface of said third stacked nonconductive substrate, each die of said plurality of fourth semiconductor dice connected to said at least one trace of said second plurality of traces of said third stacked nonconductive substrate connected to said another bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate;

a plurality of fifth semiconductor dice disposed on said second surface of said third stacked nonconductive substrate; and

a third plurality of connections connecting said third stacked nonconductive substrate and said second stacked nonconductive substrate, at least one connection of said third plurality of connections connecting said at least one bond pad of said plurality of bond pads on said first surface of said third stacked nonconductive substrate to said at least one bond pad of said plurality of bond pads on said second surface of said second stacked nonconductive substrate.

20. The assembly of claim 19, wherein said first plurality of connections and second plurality of connections each includes solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

of bond pads on said second surface of said base substrate to external electrical circuitry.